Application No. 09/836,777
Filed: April 17, 2001
TC Art Unit: 2664
Confirmation No.: 6860

REMARKS

The foregoing Amendment is filed in response to the official action dated November 30, 2004. Reconsideration is respectfully requested.

The status of the claims is as follows.

Claims 1-12 are pending in the application.

Claims 1-4, 6-8, and 10-12 stand rejected.

Claims 5 and 9 are objected to.

Claims 5 and 9 have been amended.

The Examiner has objected to the ABSTRACT of the disclosure because the ABSTRACT's word count is 154 words. The Applicant has amended the ABSTRACT to reduce the word count to 150 words or less. Further, a replacement ABSTRACT is submitted herewith on a separate sheet. Accordingly, it is respectfully submitted that the ABSTRACT, as amended, is acceptable.

The Examiner has rejected claims 1-4, 6-8, and 10-12 under 35 U.S.C. 102(e) as being anticipated by Irwin *et al.* (USP 5,841,771). Specifically, the official action indicates that the Irwin reference discloses a SONET multiplexed communications system including at least one SONET input signal path, at least one SONET output signal path, and a time slot interchange circuit, in which the SONET input signal path has a pointer interpreter for



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interpreting at least one input signal pointer serially coupled to a synchronization buffer for transferring the input signal from a respective clock rate of the input signal path to a respective clock rate of the time slot interchange circuit, and the SONET output signal path has a pointer generator for generating at least one output signal pointer serially coupled to a first-in-first-out (FIFO) buffer for transferring the output signal from the respective clock rate of the time slot interchange circuit to a respective clock rate of the output signal path. The Applicant respectfully submits, however, that the Irwin reference does not disclose each and every element/step of base claims 1, 7, and 11, and therefore the Irwin reference does not anticipate claims 1, 7, and 11 and the claims dependent therefrom.

For example, the Irwin reference does not disclose a SONET multiplexed communications system, in which a SONET input signal path has a pointer interpreter for interpreting at least one input signal and a synchronization buffer for transferring the input signal from a respective clock rate of the input signal path to a respective clock rate of a time slot interchange circuit, and a SONET output signal path has a pointer generator for generating at least one output signal pointer and a FIFO buffer for transferring the output signal from the respective clock rate of the time slot



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interchange circuit to a respective clock rate of the output signal path, as recited in claim 1.

The notion of providing a SONET multiplexed system architecture, in which each SONET input signal path includes a pointer interpreter and a synchronization buffer to compensate for timing variations in SONET input and output signals resulting from different clock rates of the input/output signal paths, and each SONET output signal path includes a FIFO buffer and a pointer generator to compensate for timing variations in the SONET input and output signals resulting from different locations of transport overhead information included in the input and output signals, is described throughout the instant application, for example, see page 3, line 21, to page 4, line 8, of the application.

Although the Irwin reference discloses that the use of queuing buffers for data switching has been a common practice for data applications (see column 13, lines 60-62, of Irwin *et al.*), the Irwin reference discloses nothing about using a synchronization buffer in combination with a pointer interpreter in a SONET input signal path, and a FIFO buffer in combination with a pointer generator in a SONET output signal path, as recited in claim 1. Instead, the Irwin reference discloses a communications facility that includes an ATM cell buffer **460**, an



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input controller **480** that generates and maintains an incoming cell management table **481**, and an output controller **490** that generates and maintains an outgoing cell management table **491** (see Figs. 5-6 of Irwin *et al.*).

Specifically, the incoming cell management table **481** includes n rows of columns A, M, N, P and D, in which A is an incoming header address which identifies data in the adjacent row, M is an asynchronous buffer write pointer which defines the next empty storage location into which the payload is to be written, N is an asynchronous buffer read pointer which defines the next of the queues in the buffer **460** for reading out a cell payload, P is a DS0 write buffer offset pointer which selects a block in DS0 buffers **428** or **429** by defining a start point in the counter **424**, and D is a delay pad parameter which defines a starting difference or space between the write pointer M and the read pointer N. Further, an outgoing cell management table **491** includes n rows of columns B, Q, R and C, in which B is an outgoing header address supplied from the controller, Q is a DS0 connection memory offset read pointer which defines the next block in the DS0 buffer **428** or **429** for randomly reading out a cell, R is an output port selection address used by the demultiplexer **412** to direct a cell to its destined line, and C is a frame scheduling flag that identifies an



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outgoing cell as having either an asynchronous cell payload or an isochronous cell payload. The function of this tabularized information in the input and output controller tables **481** and **491** is that of effecting ingress of data in ATM cells and egress of data in ATM cells while effecting SONET intraframe DS0 switching (see column 15, line 64, to column 16, line 31, and Fig. 6, of Irwin *et al.*). Significantly, the pointers in the incoming and outgoing cell management tables **481** and **491** are not employed to determine the location of data within the ATM cells, but are instead used to define storage locations in the buffer **460** into which payload data is to be written, and from which payload data is to be read (see, *e.g.*, column 16, lines 3-8, of Irwin *et al.*). In contrast, claim 1 recites that each SONET input signal path includes a pointer interpreter for interpreting at least one input signal pointer, and that each SONET output signal path includes a pointer generator for generating at least one output signal pointer.

The operation of the pointer interpreter and the pointer generator of claim 1 is therefore significantly different from that of the input and output controllers **480**, **490** and the incoming and outgoing cell management tables **481**, **491**, as disclosed in the Irwin reference. Whereas Irwin *et al.* teach that the pointers



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corresponding to the cell management tables **481**, **491** are used to define the storage locations in the buffer **460** into which payload data is to be written and from which payload data is to be read, the pointers handled by the pointer interpreter and the pointer generator of claim 1 are used in the processing of incoming and outgoing data frames. For example, as described in the instant application, each pointer interpreter is configured to interpret the H1H2 bytes to determine the pointer of the trace byte (*i.e.*, the J1 byte) pointing to the start of the SPE bytes, thereby determining the respective locations of the POH bytes, the fixed stuff bytes, and the payload data bytes in the incoming frames (see page 13, lines 1-8, of the application). As further described in the instant application, each pointer generator is configured to determine outgoing pointer values for the outgoing frames using J1 byte indications, and to perform negative/positive justifications (see page 25, lines 4-9, of the application). Clearly, the functionality of the pointer interpreter and the pointer generator, as recited in claim 1 and described in the instant application, is different from that of the input and output controllers **480**, **490** and the incoming and outgoing cell management tables **481**, **491**, as disclosed in the Irwin reference.



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Because the Irwin reference does not disclose a SONET multiplexed communications system that includes a SONET input signal path having a pointer interpreter for interpreting at least one input signal and a synchronization buffer for transferring the input signal from a respective clock rate of the input signal path to a respective clock rate of a time slot interchange circuit, and a SONET output signal path having a pointer generator for generating at least one output signal pointer and a FIFO buffer for transferring the output signal from the respective clock rate of the time slot interchange circuit to a respective clock rate of the output signal path, as recited in claim 1, the Irwin reference does not anticipate claim 1. Further, because base claims 7 and 11 also recite the pointer interpreter and the pointer generator in combination with the synchronization and FIFO buffers, the Irwin reference does not anticipate claims 7 and 11. Accordingly, it is respectfully submitted that the rejections of claims 1, 7, and 11 and the claims dependent therefrom under section 102 of the Patent Laws are unwarranted and should be withdrawn.

Specifically, with respect to dependent claims 4 and 8, the official action indicates that the Irwin reference discloses principles of time slot switching as are commonly employed in STM (synchronous time multiplex) communications networks (see column



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10, lines 42-47, of Irwin *et al.*). The Applicant respectfully points out, however, that claims 4 and 8 do not recite "STM" communications networks, but rather recite that an input signal is an "STS-M (M > 1)" signal, in which "STS-M" is an acronym relating to synchronous transport signal frames. Specifically, a SONET input signal can be formatted in STS-M frames, in which each row of the STS-M frame typically includes eighty-seven columns of SPE bytes, and each column includes M time slots of one byte each for each one of the M STS-1 tributaries (see page 8, lines 17-20, of the application). Because the mere mention of STM communications networks in the Irwin reference does not anticipate SONET signals formatted in STS-M frames, the Irwin reference does not anticipate dependent claims 4 and 8 and any claims dependent therefrom.

Claims 5 and 9 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. The Applicant has rewritten claims 5 and 9 in independent form as suggested in the official action. Accordingly, it is respectfully submitted that claims 5 and 9, as amended, should be allowed.



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In view of the foregoing, it is respectfully submitted that the present application is in a condition for allowance. Early and favorable action is respectfully requested.

The Examiner is encouraged to telephone the undersigned Attorney to discuss any matter that would expedite allowance of the present application.

Respectfully submitted,

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